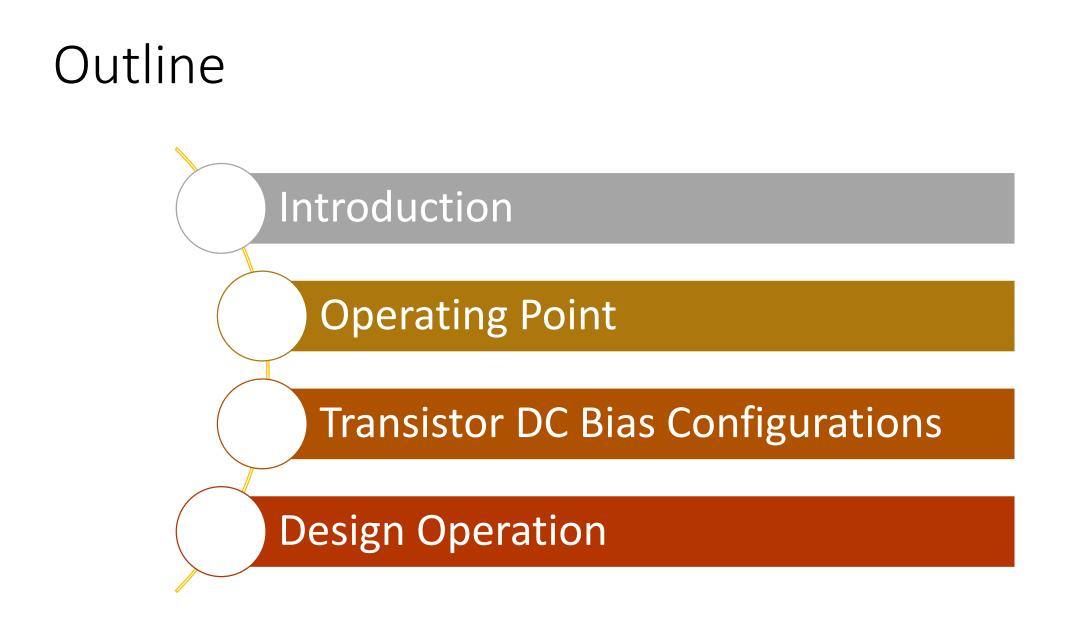
ECE 321C **Electronic Circuits** Lec. 2: BJT Biasing Circuits Instructor **Dr. Maher Abdelrasoul** http://www.bu.edu.eg/staff/mahersalem3



Introduction

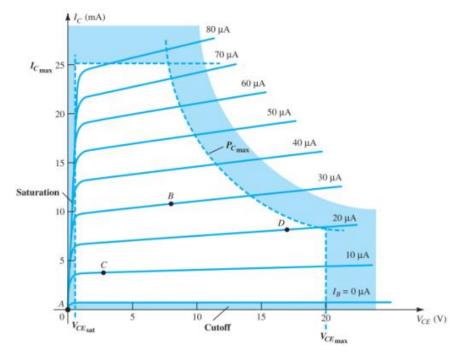
- Any increase in ac voltage, current, or power is the result of a transfer of energy from the applied dc supplies.
- The analysis or design of any electronic amplifier therefore has two components: a dc and an ac portion.
- Basic Relationships/formulas for a transistor:

$$V_{BE} \cong 0.7 \text{ V}$$
$$I_E = (\beta + 1)I_B \cong I_C$$
$$I_C = \beta I_B$$

• **Biasing** means applying of dc voltages to establish a fixed level of current and voltage. >>> Q-Point

Operating Point

- For transistor amplifiers the resulting dc current and voltage establish an operating point on the characteristics that define the region that will be employed for amplification of the applied signal.
- Because the operating point is a fixed point on the characteristics, it is also called the quiescent point (abbreviated Q-point).
- Transistor Regions Operation:
 - Linear-region operation: Base–emitter junction forward-biased Base–collector junction reverse-biased
 - Cutoff-region operation:
 Base–emitter junction reverse-biased
 Base–collector junction reverse-biased
 - Saturation-region operation:
 Base-emitter junction forward-biased
 Base-collector junction forward-biased



Transistor DC Bias Configurations

✓ Fixed-Bias Configuration

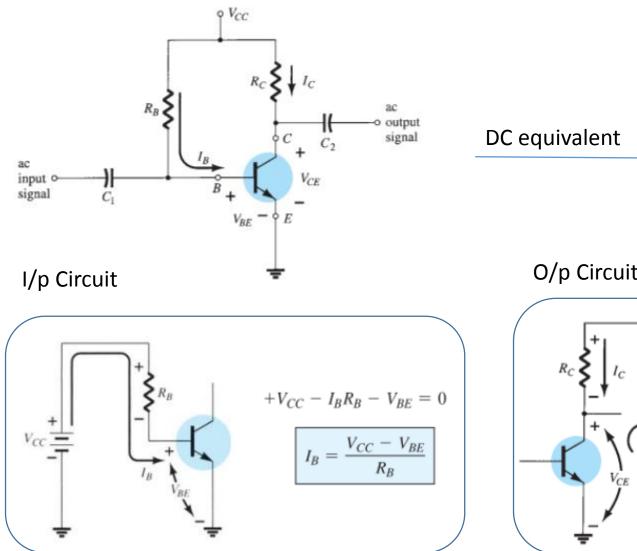
✓ Emitter-Bias Configuration

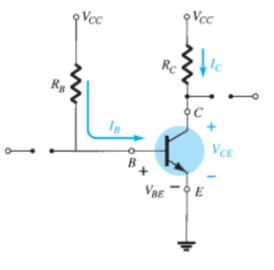
✓Voltage-Divider Bias Configuration

✓ Collector Feedback Configuration

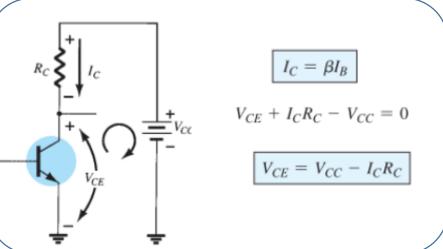
- ✓ Emitter-Follower Configuration
- ✓ Common-Base Configuration
- ✓ Miscellaneous Bias Configurations

Fixed-Bias Configuration (1 of 4)









Fixed-Bias Configuration (2 of 4)

EXAMPLE 4.1 Determine the following for the fixed-bias configuration

a. I_{B_Q} and I_{C_Q} . b. V_{CE_Q} . c. V_B and V_C . d. V_{BC} .

Solution:

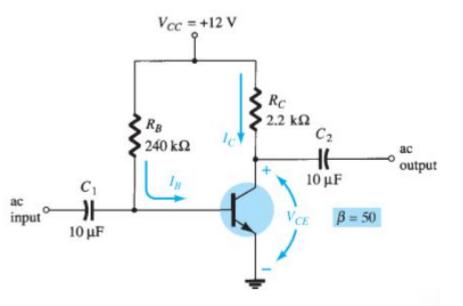
$$I_{B_Q} = \frac{V_{CC} - V_{BE}}{R_B} = \frac{12 \text{ V} - 0.7 \text{ V}}{240 \text{ k}\Omega} = 47.08 \ \mu\text{A}$$
$$I_{C_Q} = \beta I_{BQ} = (50)(47.08 \ \mu\text{A}) = 2.35 \text{ mA}$$
$$V_{CE_Q} = V_{CC} - I_C R_C$$
$$= 12 \text{ V} - (2.35 \text{ mA})(2.2 \text{ k}\Omega)$$
$$= 6.83 \text{ V}$$
$$V_R = V_{RE} = 0.7 \text{ V}$$

 $V_C = V_{CE} = 6.83 \text{ V}$ Using double-subscript notation yields

$$V_{BC} = V_B - V_C = 0.7 \text{ V} - 6.83 \text{ V}$$

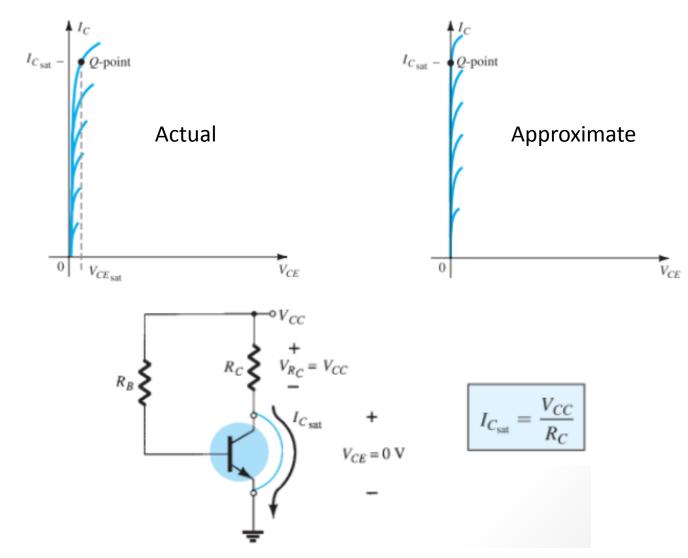
= -6.13 V

with the negative sign revealing that the junction is reversed-biased, as it should be for linear amplification.



Fixed-Bias Configuration (3 of 4)

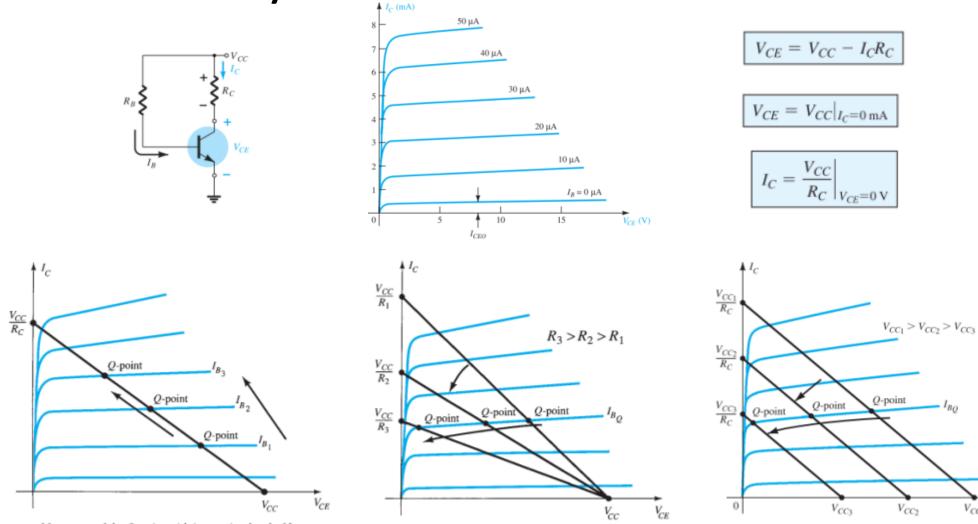
Transistor Saturation



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Fixed-Bias Configuration (4 of 4)

Load Line Analysis



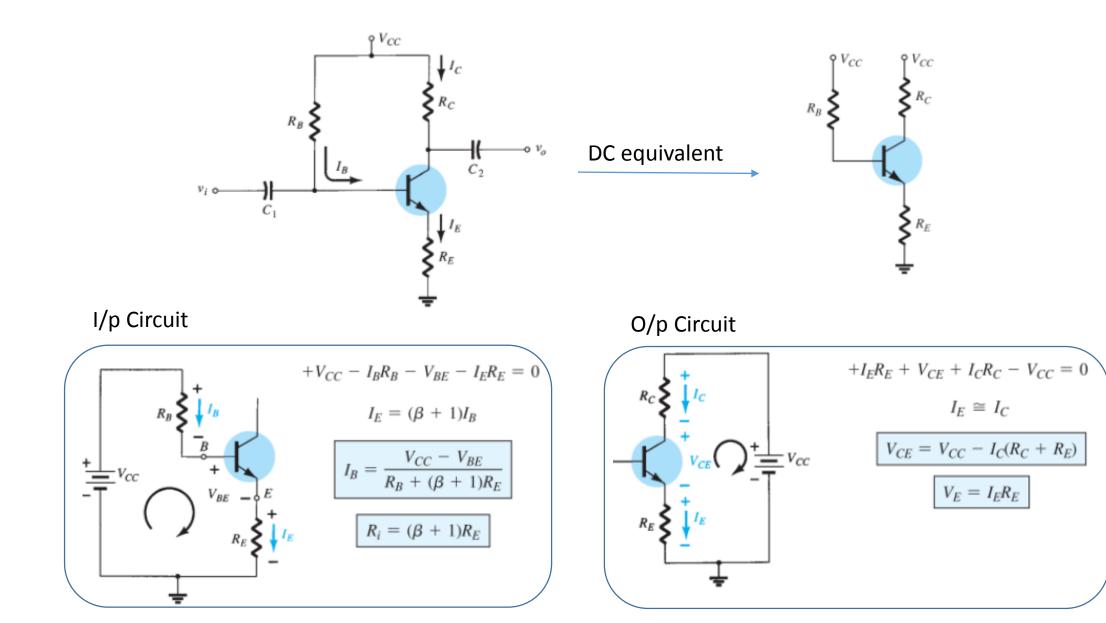
Movement of the Q-point with increasing level of IB.

Effect of an increasing level of R_C on the load line and the Q-point.

 V_{CC_1}

 V_{CE}

Emitter-Bias Configuration (1 of 4)



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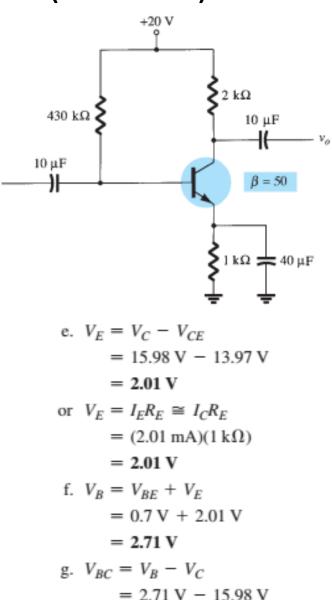
Emitter-Bias Configuration (2 of 4)



a. I_B . e. V_E . b. I_C . f. V_B . c. V_{CE} . g. V_{BC} . d. V_C .

Solution:

a. Eq. (4.17): $I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_E} = \frac{20 \text{ V} - 0.7 \text{ V}}{430 \text{ k}\Omega + (51)(1 \text{ k}\Omega)}$ $= \frac{19.3 \text{ V}}{481 \text{ k}\Omega} = 40.1 \mu\text{A}$ b. $I_C = \beta I_B$ $= (50)(40.1 \mu\text{A})$ $\cong 2.01 \text{ mA}$ c. Eq. (4.19): $V_{CE} = V_{CC} - I_C(R_C + R_E)$ $= 20 \text{ V} - (2.01 \text{ mA})(2 \text{ k}\Omega + 1 \text{ k}\Omega) = 20 \text{ V} - 6.03 \text{ V}$ = 13.97 Vd. $V_C = V_{CC} - I_C R_C$ $= 20 \text{ V} - (2.01 \text{ mA})(2 \text{ k}\Omega) = 20 \text{ V} - 4.02 \text{ V}$ = 15.98 V



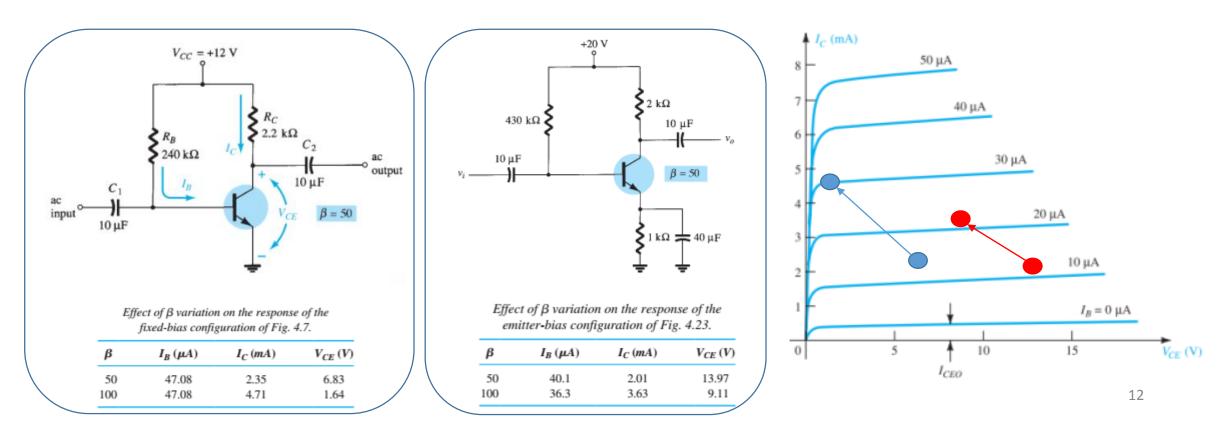
= -13.27 V (reverse-biased as required)

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Emitter-Bias Configuration (3 of 4)

• Improved Bias Stability

The addition of the emitter resistor to the dc bias of the BJT provides improved stability, that is, the dc bias currents and voltages remain closer to where they were set by the circuit when outside conditions, such as temperature and transistor beta, change.



Emitter-Bias Configuration (4 of 4)

Saturation Level

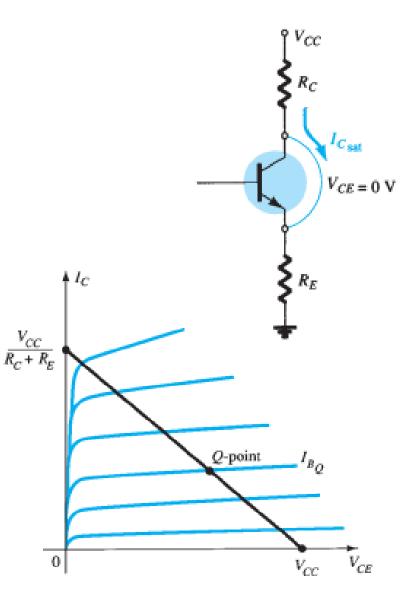
$$I_{C_{\rm sat}} = \frac{V_{CC}}{R_C + R_E}$$

Load-Line Analysis

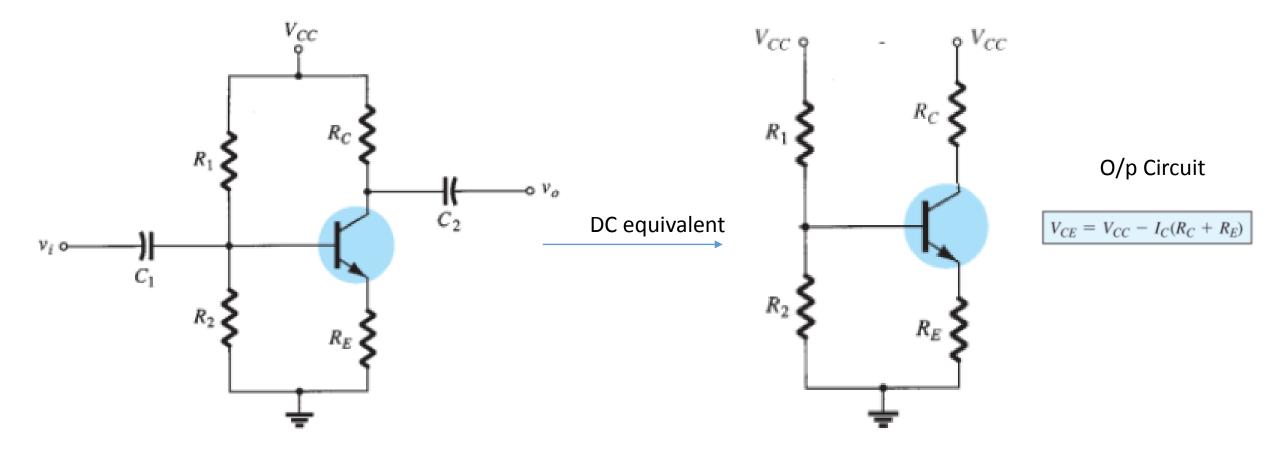
$$V_{CE} = V_{CC} - I_C(R_C + R_E)$$

$$V_{CE} = V_{CC} |_{I_C = 0 \text{ mA}}$$

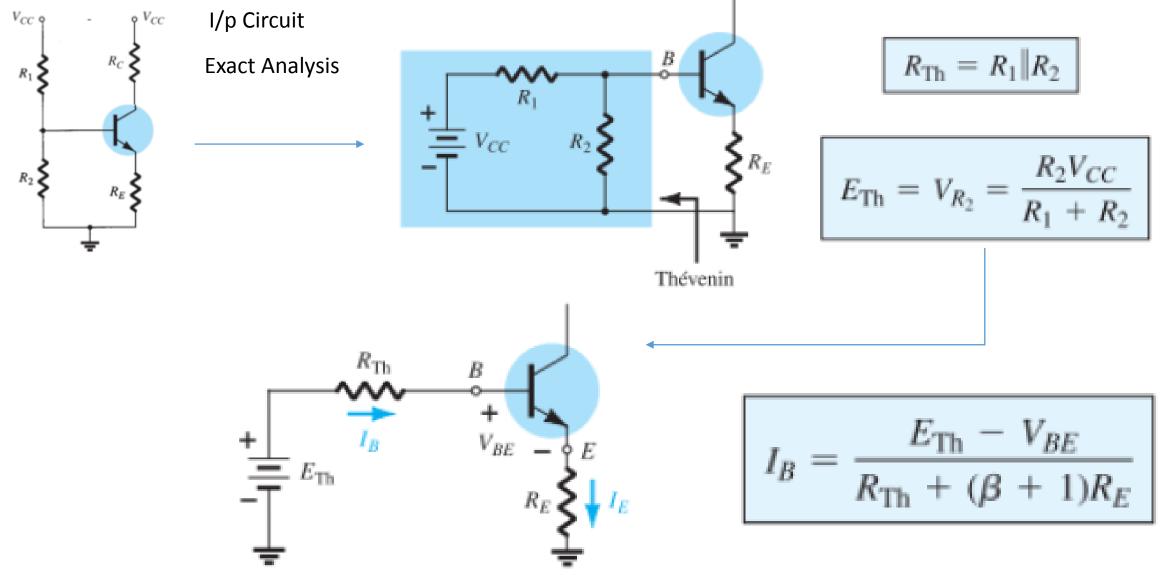
$$I_C = \frac{V_{CC}}{R_C + R_E} \Big|_{V_{CE} = 0 \text{ V}}$$



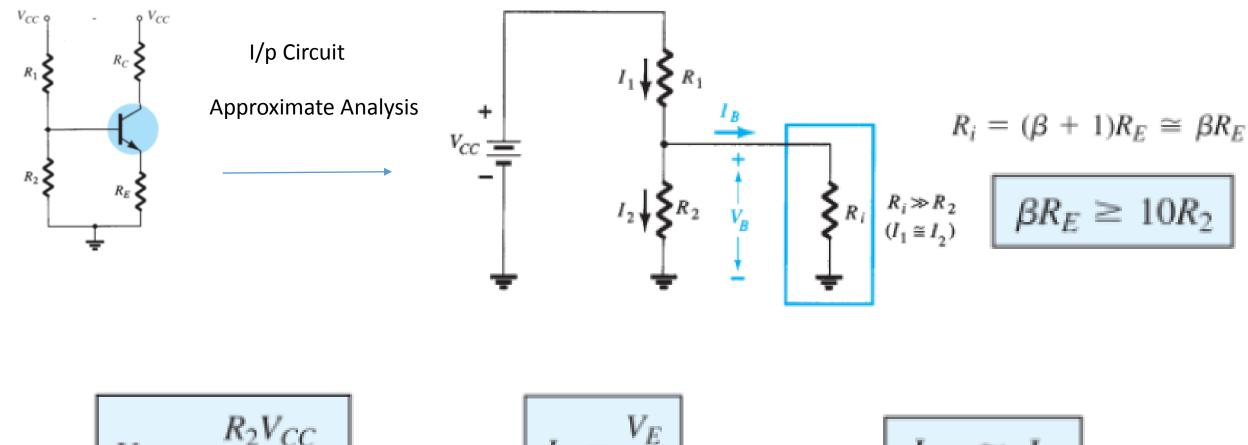
Voltage-Divider Configuration (analysis)₁



Voltage-Divider Configuration (analysis)₂



Voltage-Divider Configuration (analysis)₃



$$V_B = \frac{R_2 V_{CC}}{R_1 + R_2}$$

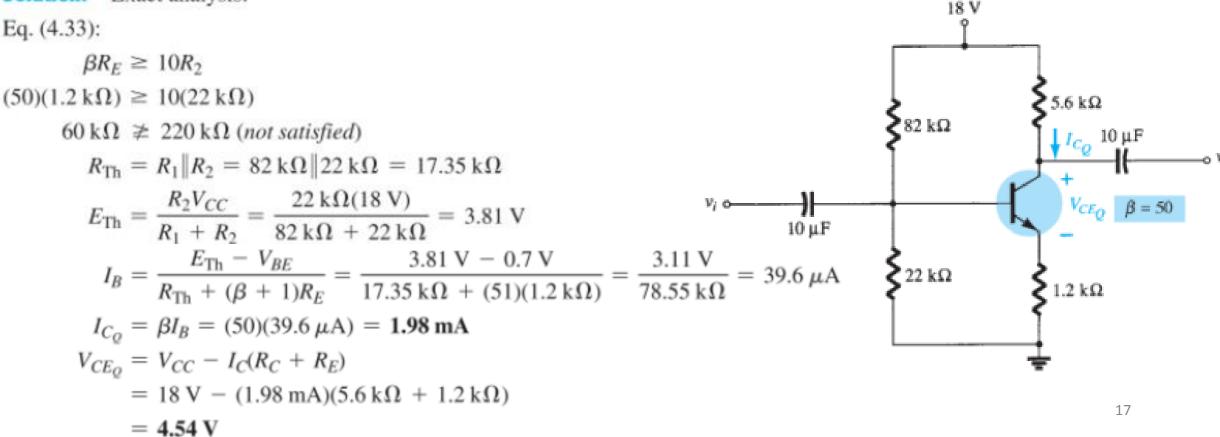
$$I_E = \frac{V_E}{R_E}$$

$$I_{C_Q} \cong I_E$$

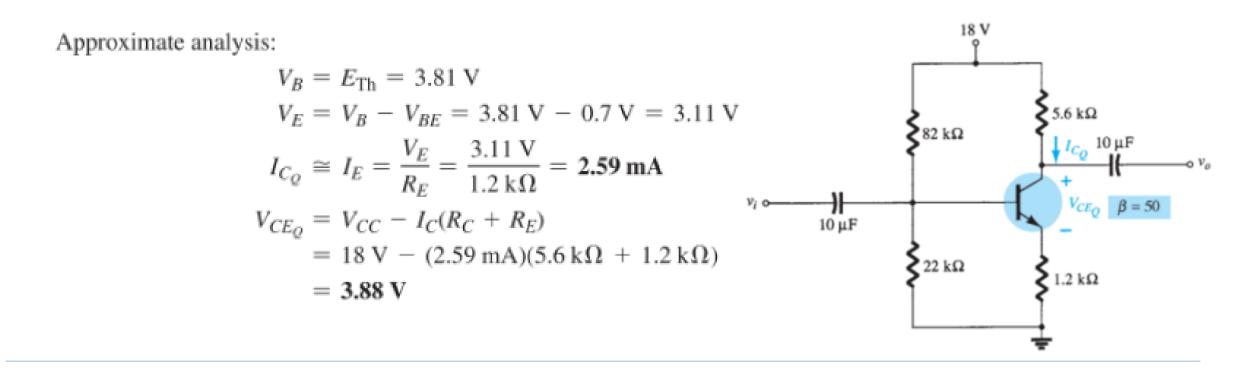
Voltage-Divider Configuration (Example)₁

EXAMPLE 4.11 Determine the levels of I_{C_Q} and V_{CE_Q} for the voltage-divider configuration of Fig. 4.37 using the exact and approximate techniques and compare solutions. In this case, the conditions of Eq. (4.33) will not be satisfied and the results will reveal the difference in solution if the criterion of Eq. (4.33) is ignored.

Solution: Exact analysis:



Voltage-Divider Configuration (Example)₂



	$I_{C_Q}(mA)$	$V_{CE_Q}(V)$
Exact	1.98	4.54
Approximate	2.59	3.88

Comparing the exact and approximate approaches.

To ensure a close similarity between exact and approximate solutions.

$$\beta R_E \ge 10R_2$$

Voltage-Divider Configuration (Load-Line)

Saturation Level

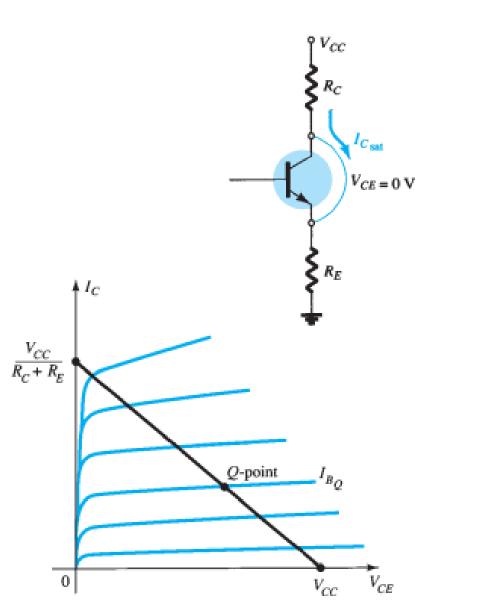
$$I_{C_{\rm sat}} = \frac{V_{CC}}{R_C + R_E}$$

Load-Line Analysis

$$V_{CE} = V_{CC} - I_C(R_C + R_E)$$

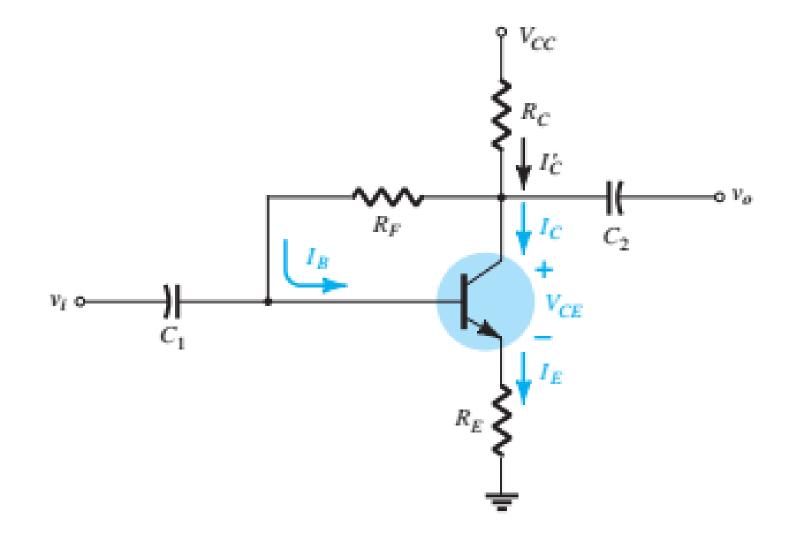
$$V_{CE} = V_{CC} |_{I_C = 0 \text{ mA}}$$

$$I_C = \frac{V_{CC}}{R_C + R_E} \bigg|_{V_{CE} = 0 \text{ V}}$$

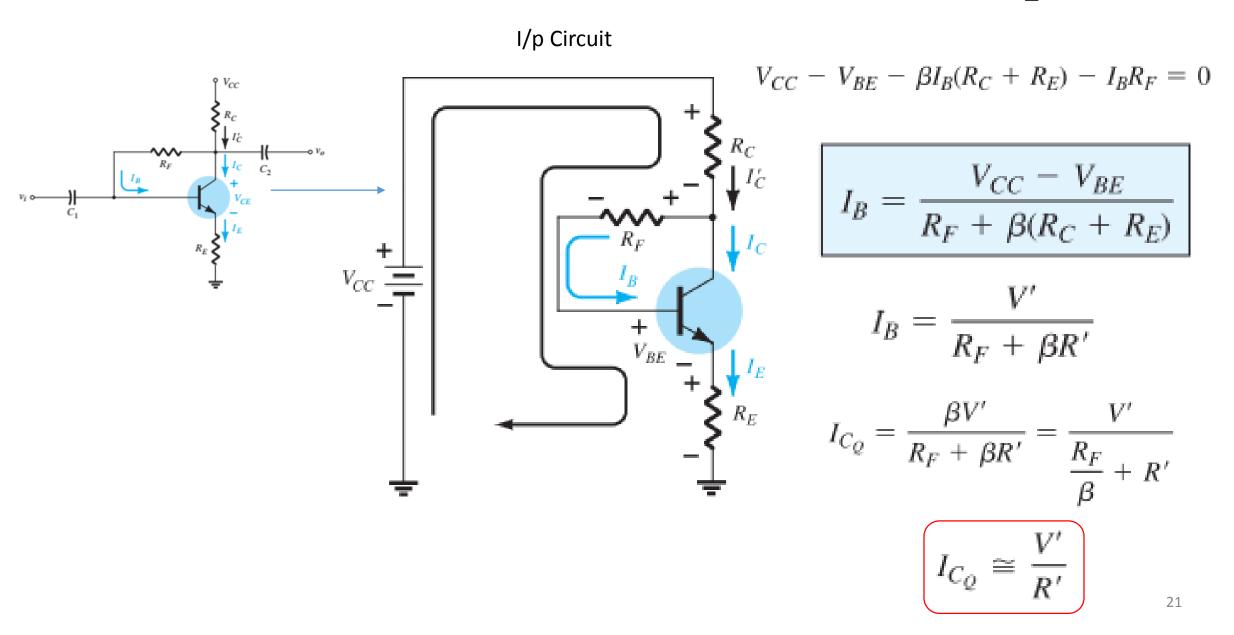


Collector Feedback Configuration (Analysis)₁

• DC bias circuit with voltage feedback.

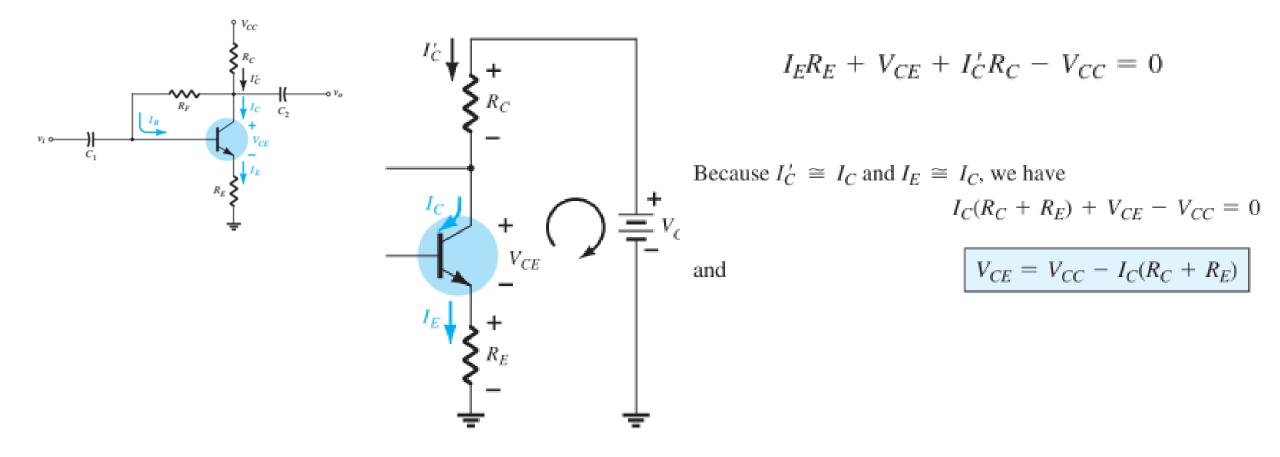


Collector Feedback Configuration (Analysis)₂



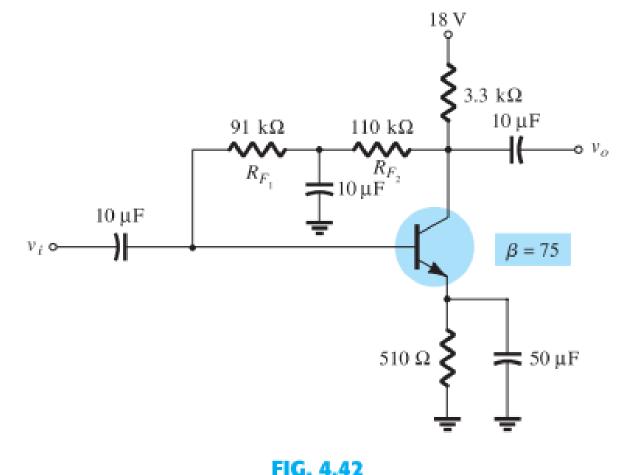
Collector Feedback Configuration (Analysis)₁

O/p Circuit



Collector Feedback Configuration (Example)₁

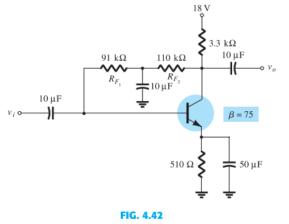
EXAMPLE 4.14 Determine the dc level of I_B and V_C for the network of Fig. 4.42.

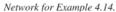


Network for Example 4.14.

Collector Feedback Configuration (Example)₁

EXAMPLE 4.14 Determine the dc level of I_B and V_C for the network of Fig. 4.42.





Solution: In this case, the base resistance for the dc analysis is composed of two resistors with a capacitor connected from their junction to ground. For the dc mode, the capacitor assumes the open-circuit equivalence, and $R_B = R_{F_1} + R_{F_2}$. Solving for I_B gives

$$I_{B} = \frac{V_{CC} - V_{BE}}{R_{B} + \beta(R_{C} + R_{E})}$$

$$= \frac{18 \text{ V} - 0.7 \text{ V}}{(91 \text{ k}\Omega + 110 \text{ k}\Omega) + (75)(3.3 \text{ k}\Omega + 0.51 \text{ k}\Omega)}$$

$$= \frac{17.3 \text{ V}}{201 \text{ k}\Omega + 285.75 \text{ k}\Omega} = \frac{17.3 \text{ V}}{486.75 \text{ k}\Omega}$$

$$= 35.5 \,\mu\text{A}$$

$$I_{C} = \beta I_{B}$$

$$= (75)(35.5 \,\mu\text{A})$$

$$= 2.66 \text{ mA}$$

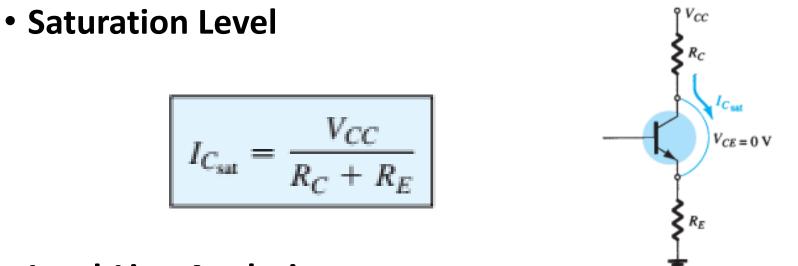
$$V_{C} = V_{CC} - I'_{C}R_{C} \cong V_{CC} - I_{C}R_{C}$$

$$= 18 \text{ V} - (2.66 \text{ mA})(3.3 \text{ k}\Omega)$$

$$= 18 \text{ V} - 8.78 \text{ V}$$

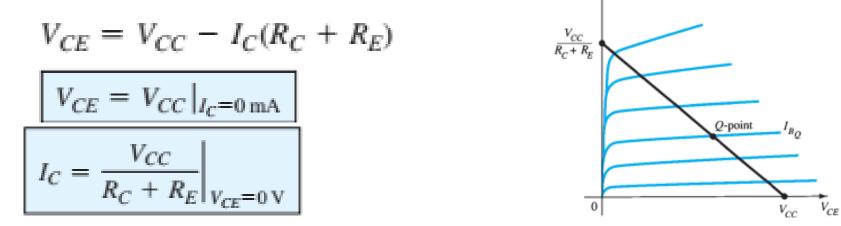
$$= 9.22 \text{ V}$$

Collector Feedback Configuration (Load-Line)

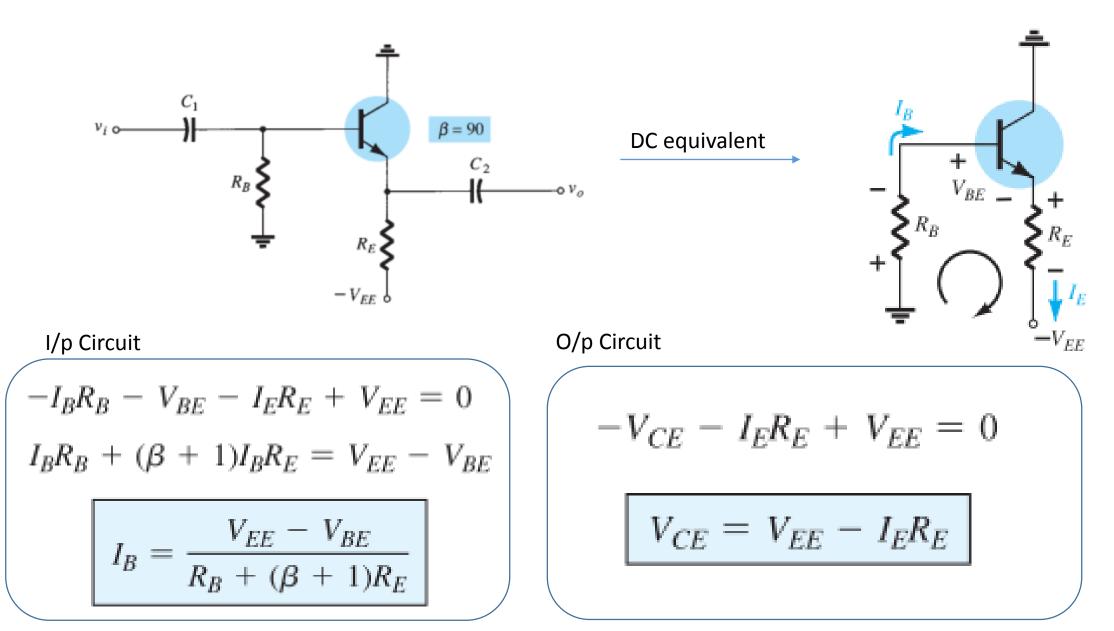


Load-Line Analysis

Continuing with the approximation $I'_{c} = I_{c}$ results in the same load line defined for the voltage-divider and emitter-biased configurations.

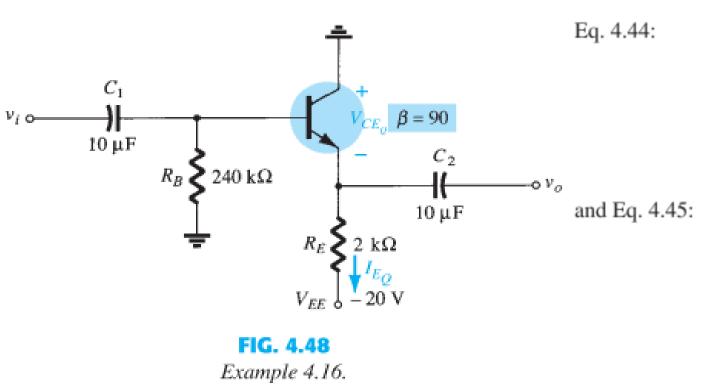


Emitter-Follower Configuration (analysis)



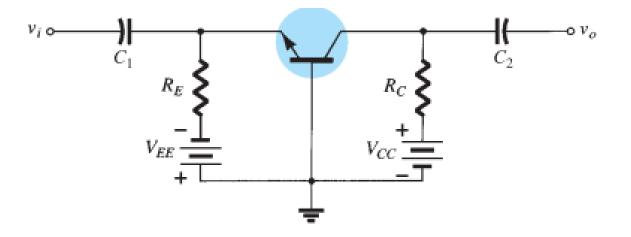
Emitter-Follower Configuration (Example)

Determine V_{CE_0} and I_{E_0} for the network of Fig. 4.48.

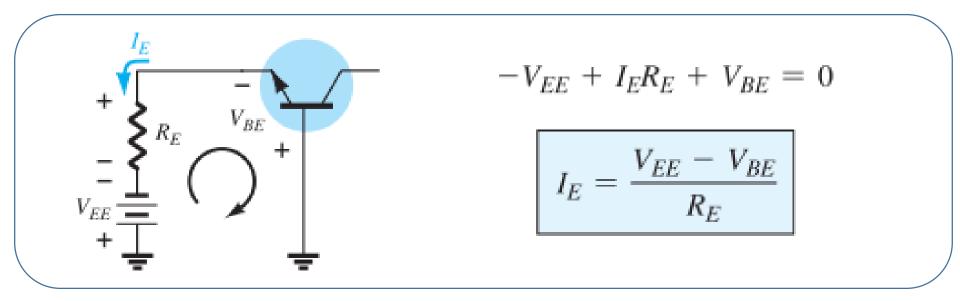


$$\begin{split} I_B &= \frac{V_{EE} - V_{BE}}{R_B + (\beta + 1)R_E} \\ &= \frac{20 \text{ V} - 0.7 \text{ V}}{240 \text{ k}\Omega + (90 + 1)2 \text{ k}\Omega} = \frac{19.3 \text{ V}}{240 \text{ k}\Omega + 182 \text{ k}\Omega} \\ &= \frac{19.3 \text{ V}}{422 \text{ k}\Omega} = 45.73 \,\mu\text{A} \\ V_{CE_Q} &= V_{EE} - I_E R_E \\ &= V_{EE} - (\beta + 1)I_B R_E \\ &= 20 \text{ V} - (90 + 1)(45.73 \,\mu\text{A})(2 \text{ k}\Omega) \\ &= 20 \text{ V} - 8.32 \text{ V} \\ &= 11.68 \text{ V} \\ I_{E_Q} &= (\beta + 1)I_B = (91)(45.73 \,\mu\text{A}) \\ &= 4.16 \text{ mA} \end{split}$$

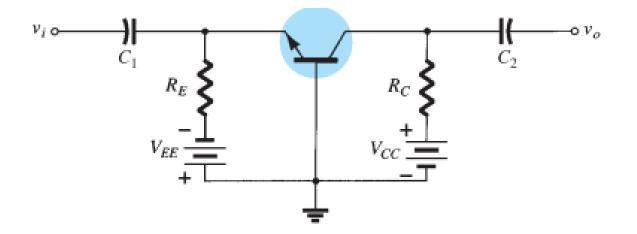
Common-Base Configuration (analysis)₁



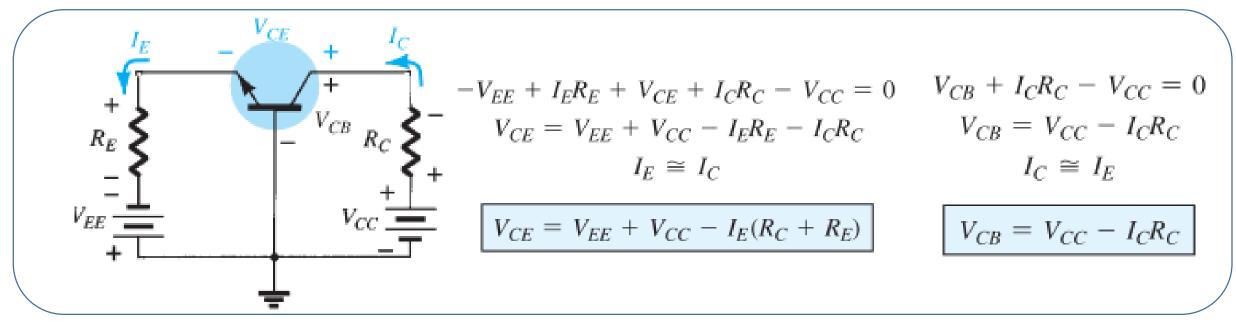
I/p Circuit



Common-Base Configuration (analysis)

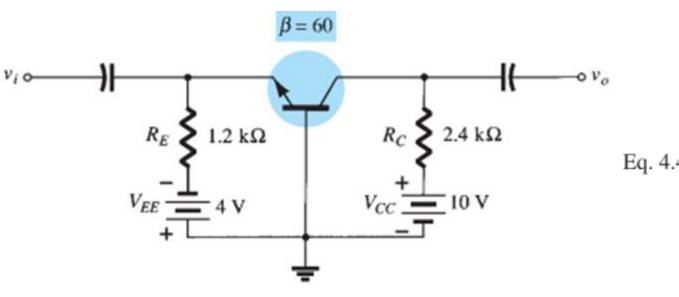


O/p Circuit



Common-Base Configuration (Example)

EXAMPLE 4.17 Determine the currents I_E and I_B and the voltages V_{CE} and V_{CB} for the common-base configuration of Fig. 4.52.



Solution: Eq. 4.46:

$$I_E = \frac{V_{EE} - V_{BE}}{R_E}$$

$$= \frac{4 \text{ V} - 0.7 \text{ V}}{1.2 \text{ k}\Omega} = 2.75 \text{ mA}$$

$$I_B = \frac{I_E}{\beta + 1} = \frac{2.75 \text{ mA}}{60 + 1} = \frac{2.75 \text{ mA}}{61}$$

$$= 45.08 \,\mu\text{A}$$
Eq. 4.47:

$$V_{CE} = V_{EE} + V_{CC} - I_E(R_C + R_E)$$

$$= 4 \text{ V} + 10 \text{ V} - (2.75 \text{ mA})(2.4 \text{ k}\Omega + 1.2 \text{ k}\Omega)$$

$$= 14 \text{ V} - (2.75 \text{ mA})(3.6 \text{ k}\Omega)$$

$$= 14 \text{ V} - 9.9 \text{ V}$$

$$= 4.1 \text{ V}$$
Eq. 4.48:

$$V_{CB} = V_{CC} - I_C R_C = V_{CC} - \beta I_B R_C$$

$$= 10 \text{ V} - (60)(45.08 \,\mu\text{A})(24 \text{ k}\Omega)$$

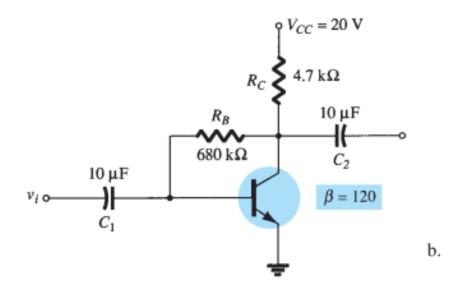
$$= 10 \text{ V} - 6.49 \text{ V}$$

$$= 3.51 \text{ V}$$

Miscellaneous Bias Configurations (1 of 2)

EXAMPLE 4.18 For the network of Fig. 4.53:

a. Determine I_{CQ} and V_{CEQ}.
b. Find V_B, V_C, V_E, and V_{BC}.



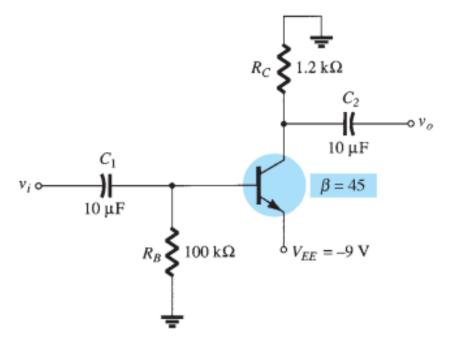
Solution:

a. The absence of R_E reduces the reflection of resistive levels to simply that of R_C , and the equation for I_B reduces to

$$I_{B} = \frac{V_{CC} - V_{BE}}{R_{B} + \beta R_{C}}$$

= $\frac{20 \text{ V} - 0.7 \text{ V}}{680 \text{ k}\Omega + (120)(4.7 \text{ k}\Omega)} = \frac{19.3 \text{ V}}{1.244 \text{ M}\Omega}$
= $15.51 \mu \text{A}$
 $I_{C_{Q}} = \beta I_{B} = (120)(15.51 \mu \text{A})$
= 1.86 mA
 $V_{CE_{Q}} = V_{CC} - I_{C}R_{C}$
= $20 \text{ V} - (1.86 \text{ mA})(4.7 \text{ k}\Omega)$
= 11.26 V
 $V_{B} = V_{BE} = 0.7 \text{ V}$
 $V_{C} = V_{CE} = 11.26 \text{ V}$
 $V_{E} = 0 \text{ V}$
 $V_{BC} = V_{B} - V_{C} = 0.7 \text{ V} - 11.26 \text{ V}$
= -10.56 V

Miscellaneous Bias Configurations (2 of 2) EXAMPLE 4.19 Determine V_C and V_B for the network of Fig. 4.54.



Solution: Applying Kirchhoff's voltage law in the clockwise direction for the base-emitter loop results in

and

$$-I_B R_B - V_{BE} + V_{EE} = 0$$
$$I_B = \frac{V_{EE} - V_{BE}}{R_B}$$

Substitution yields

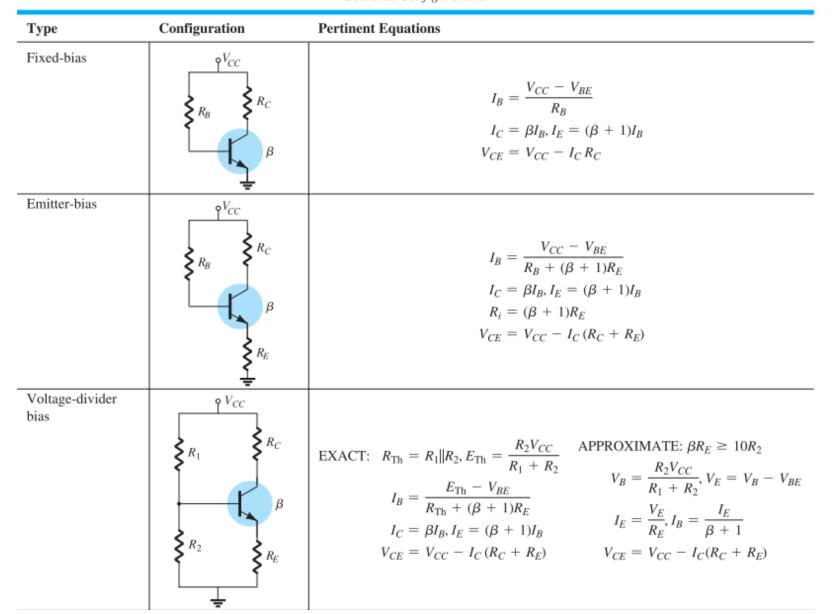
$$I_B = \frac{9 \text{ V} - 0.7 \text{ V}}{100 \text{ k}\Omega}$$
$$= \frac{8.3 \text{ V}}{100 \text{ k}\Omega}$$
$$= 83 \mu\text{A}$$

 $I_C = \beta I_B$ $= (45)(83 \,\mu A)$ $= 3.735 \,\mathrm{mA}$ $V_C = -I_C R_C$ $= -(3.735 \text{ mA})(1.2 \text{ k}\Omega)$ = -4.48 V $V_B = -I_B R_B$ $= -(83 \,\mu A)(100 \,k\Omega)$ = -8.3 V

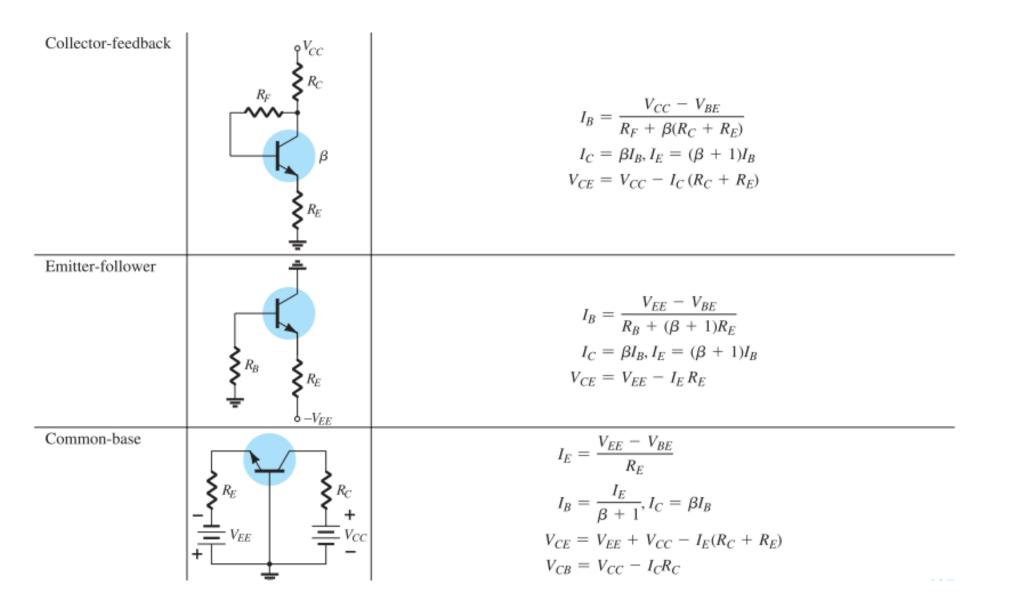
32

Summary Table

BJT Bias Configurations



Summary Table..



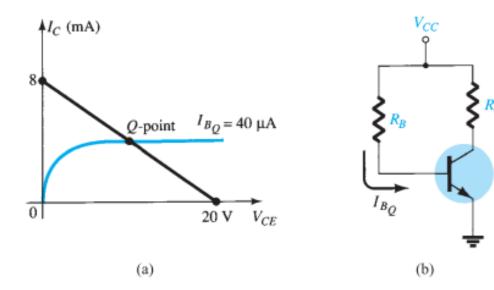
Design Operation

Design Operations

- Discussions thus far have focused on the analysis of existing networks. All the elements are in place, and it is simply a matter of solving for the current and voltage levels of the configuration.
- The design process is one where a current and/or voltage may be specified and the elements required to establish the designated levels must be determined.
- The design sequence is obviously sensitive to the components that are already specified and the elements to be determined. If the transistor and supplies are specified, the design process will simply determine the required resistors for a particular design.
- Once the theoretical values of the resistors are determined, the nearest standard commercial values are normally chosen and any variations due to not using the exact resistance values are accepted as part of the design.

Design Operations Example

EXAMPLE 4.21 Given the device characteristics of Fig. 4.59a, determine V_{CC} , R_B , and R_C **Solution:** From the load line for the fixed-bias configuration of Fig. 4.59b.



and

with

 $V_{CC} = 20 \text{ V}$ $I_C = \frac{V_{CC}}{R_C} \bigg|_{V_{CE} = 0 \text{ V}}$ $R_C = \frac{V_{CC}}{I_C} = \frac{20 \text{ V}}{8 \text{ mA}} = 2.5 \text{ k}\Omega$ $I_B = \frac{V_{CC} - V_{BE}}{R_B}$ $R_B = \frac{V_{CC} - V_{BE}}{I_B}$ $=\frac{20 \text{ V} - 0.7 \text{ V}}{40 \,\mu\text{A}} = \frac{19.3 \text{ V}}{40 \,\mu\text{A}}$ $= 482.5 \,\mathrm{k}\Omega$

Standard resistor values are

 $R_C = 2.4 \,\mathrm{k}\Omega$ $R_B = 470 \,\mathrm{k}\Omega$

Using standard resistor values gives

$$I_B = 41.1 \, \mu A$$

which is well within 5% of the value specified. ³⁷

